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From Mainstay Boards to Highest Tech Eagle Electronics is Poised for Flight

From its beginning in 1979, Eagle Electronics (Schaumburg, IL) has specialized in high-volume PCBs. Today, its capabilities have broadened, its customers are global, and its main driver is value-added repeat business. It has proven itself well-able to manage the market swings, technology disruptions and general chaos that has accompanied 4 decades of board building in an insanely competitive environment.

While high-volume projects remain a mainstay, Eagle has also established the infrastructure and processes to pursue highly advanced board designs. "Blind and buried vias, stacked and staggered microvias, plated cavities, metal core boards for LEDs, 40-layer, and boards with a thickness up to .250 inches," says Eagle Director of Sales and Marketing, Andy D'Agostino, "this is where we proved ourselves following the 2001 telecom crash."

Eagle Electronics is Poised for Flight, continued

AOI inspection of an inner laver

The transformation happened in stages. "Asia started to push sales here in the late 90s, with suppliers first from Taiwan, then China. The question for us was, did we want to go to the 'broker' model, or change our production model?

"Ownership decided to re-tool, and re-equip, expanding our capabilities from exclusively single and doublesided boards to quick-turn and high tech work that was more in line with the technology needed for prototype builds.

"We really pushed the technology bandwidth within Eagle after 2001, investing heavily in people and equipment for HDI production." Eagle's move toward higher tech boards received an unexpected boost when Rob Coleman, a long-time supplier to Eagle, joined Uyemura in 2016. One of his first calls was to Brett McCoy, the COO. "What have you got?" McCoy asked. "A copper via fill," Coleman replied, "called EVF-R." Eagle was evaluating other suppliers for via fill who, according to McCoy, "could not meet Eagle's requirements."

"McCoy handed me 6 panels," recalls Coleman, "and told me we had one opportunity to deliver." At the time, Eagle was filling micro vias with a conductive ink and not getting consistent 100% fill. The issue was becoming more urgent, because microvias were shrinking. (6 mil vias were typical at the time.)

"We were interested in copper as an alternative to make the holes more robust and eliminate the trapped air that, in absence of sufficient vacuum, sometimes prevented 100% fill," explains Eagle Process Engineer Harshit Shah.

EVF-R is a unique DC acid copper plating system for filling blind vias, "It's well suited to projects where we're stacking 2-3 deep - 6 layers total," says D'Agostino. EVF-R is designed to plate aspect ratios of 1:1 or less. With current time manipulation, the EVF-R system plates void-free aspect ratios up to 1 to 1:2.

EPIG Opens Wide Avenue for HF, Designs with Reduced Spacing

EPIG (Electroless Palladium, Immersion Gold) is the nickel-free PCB finish that's gold wire bondable, solderable, and ideal for HF use.

UIC's EPIG process deposits palladium directly onto copper. Eliminating the nickel means less build-up on circuits, and circuits can be controlled with smaller geometries.

EPIG offers unique and significant advantages for microwave, flex circuits, and high purity applications:

- Wide operating window for gold deposition: 4-12 µin.
- No nickel to fracture on bending for flex circuits
- Short process cycle
- No skin effect on low current, HF applications
- Non-magnetic
- Suitable for tight lines and spaces
- Easy to visually inspect
- Reworkable in most instances

EVF-R is a combination of organic additives that work with a specific acid-to-copper ratio. The components include a brightener (accelerator/ grain refiner), a carrier (a wide range suppressor) and a leveler (a unique surface suppressor). Components are readily analyzable by CVS.

For best performance, the chemistry is augmented with solution dynamics that preferentially maintain the leveling component at the surface. Suppressing plating on the surface causes plating to accelerate in the bottom of the via.

ASF and dwell time are calculated according to the degree of difficulty (i.e. hole diameter vs. depth). For some projects, increasing the current density at the back end of the plating cycle is helpful.

Coleman contacted a Uyemura colleague in Minnesota and arranged to have Eagle's boards processed with EVF-R. "The results," says McCoy, "were perfect. I told

Coleman I wanted the exact same tank set-up here as in Minnesota." Coleman found a local tank supplier, and UIC National Accounts Manager for Technology George Milad generated the specifications.

Eagle's copper via fill process was installed during the 2016 Christmas shut-down. "The first board out replicated exactly what we had seen from the shop in Minnesota," says McCoy. "We never looked back."

EVF-R made possible board quality that significantly enhanced Eagle's competitive position, according to Harshit Shah. "It is most helpful when we're doing 2 mil lines with 2 mil spacing, because the process gives us better room for control of surface copper. The result is holes that are more robust, and a resulting higher reliability product. When you can fill 100% consistently, there's no worry about issues in assembly."

Higher tech products take longer to build, yet customers still demand the same turn-around as double-sided boards, according to D'Agostino. "It's like building 5 double-sided boards into one, yet there's no accommodation for that level of complexity. Products like EVF-R, along with faster drills, have helped us get our times down, and made us more competitive. We've been able to streamline the entire via fill process from 24 hours to just 3 to 3-1/2 hours."

Eagle continues to run conductive (and non-conductive) epoxy lines. "These are 24 hour processes with many more steps, but some products allow for that," explains D'Agostino. "When there are buried vias and microvias, though, it's all copper via fill." The decider is hole size: "The cut-off for copper fill is an aspect ratio of 1 to 1.2," explains Shah. "Anything beyond that uses the traditional epoxy via fill. The tighter the aspect ratio, the more compelling the case for copper via fill."

70% of Eagle's work today is ENIG processing. (ENEPIG is also offered.) The company has used the Uyemura process since 2006. "The UIC ENIG is robust and predictable," says D'Agostino, "but accommodating as well." Explains Shah, "We've experimented with variations in agitation cycles, and customized our oxidation removal techniques to improve nickel

Uyemura EVF-R Cu via fill tank



Visual inspection by an operator

acceptance. In the latter case, our method was unique at the time; today, it's regarded as an industry best practice."

Eagle maintains a full quality lab for testing board quality and chemistry. Whether the need is analysis verification for a process run as specified, or support for experiments with process variables, Eagle takes full advantage of Uyemura lab support. Uyemura is distinctive among major suppliers of PCB chemistry in providing lab support for customers without added cost.

"What matters most," says D'Agostino, "is whether we can make it in time, reliably and repeatably, and at a competitive operating cost per plated sq. ft. We've proven that we can." Eagle boards have a customer acceptance rate of 99.7%.

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Eagle's Business has grown 35% in 2018, thanks to both larger order sizes and new customers from all sectors: medical, commercial, consumables, military. "Tighter densities, continued smaller packages, and more higher tech boards are the future," he continues, "and we can now build 98% of what the market wants. That includes high frequency boards with Rogers, NELCO, and Megtron laminate systems. *Our goal is to stay 1-2 steps ahead of what our customers need.*"

In addition to via fill and ENIG, UIC supplies board shops with ENEPIG and EPIG, electroless copper, direct metallization for higher aspect ratios, and high throw acid coppers.

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Left to Right: Brett McCoy, Andy D'Agostino, Mike Kalaria, Harshit Shah

CORROSION MONITORING is Latest Requirement of 4552 Rev A

IPC ENIG Specification 4552 Rev A, released in 2016, set new limits for immersion gold thickness $(1.6 - 4.0 \mu ins)$ and introduced the "Corrosion Chart" as a reference document, to differentiate between acceptable and rejectable levels of corrosion.

IPC ENIG Specification 4552 Rev A with Amendment 1 will be issued this year. It defines the corrosion chart in greater detail and sets corrosion monitoring as a requirement for meeting the specification.

Under normal conditions, ENIG produces a corrosion-free nickel deposit, characterized by a uniform appearance of nickel under magnification (3000X), with no pronounced grain boundaries.

ENIG has several steps, any of which can produce a compromised non-uniform nickel deposit that would be susceptible to corrosion. Here are the major causes of a non-uniform nickel deposit.

- Inadequate pre-treatment
- Uneven catalyst deposition
- Ni rate of deposition too high
- Soldermask leaching into the Ni bath
- Higher MTO
- Extended dwell time (attempting to deposit more gold in an immersion bath) in an aggressive immersion gold bath (acidic pH <5.5, gold concentration below the recommended spec)

Manufacturers who understand the complexity of the ENIG process assign a competent engineer to oversee the process and an experienced operator to run and monitor the line. The process is backed by an analytical lab that maintains and documents the process variables to meet vendor specifications.

Corrosion Monitoring

A corrosion evaluation ensures that good product that exhibits minor corrosion is not rejected and that product



with excessive corrosion is rejected outright. Corrosion evaluation offers a way of characterizing the ENIG process and its capabilities throughout the life of the nickel bath.

The 3-Level Corrosion Chart

Corrosion evaluation is done by examining a cross section at 1000X. 1000X is widely available and does not require SEM magnification. It entails counting and measuring corrosion defects in the field of view. Corrosion evaluation quantifies the depth and frequency of "corrosion spikes," "corrosion spreader spikes" and "corrosion continuous black band." Each of these evaluation features is defined in great detail in the document.

Level 1 Minimum corrosion: parts are acceptable Level 2 Corrosion conditions are neither Level 1 nor Level 3. Parts may be acceptable if successful solderability is demonstrated.

Level 3 Excessive corrosion: parts are rejectable

The Corrosion Chart as specified in the 4552A allows a manufacturer to identify corrosion at its onset and take corrective action before excessive defective product is produced. It also ensures that cause is understood and corrective action is implemented.



George Milad, UIC National Accounts Manager for Technology, has 25+ years experience in PCB manufacturing. He is the recipient of the coveted IPC Presidents Award for his leadership and significant industry contributions.

Examples of Corrosion Levels (0, 1, 2, & 3)



Defect-free ENIG: No Corrosion



Level 1, Nickel Corrosion



Level 2, Nickel Corrosion



Level 3, Nickel Corrosion

Diverse Factors Contribute to Success of UIC ENEPIG

You may remember reading, in the spring issue of *Clear Signals*, about Micron's decision to specify the Uyemura ENEPIG process.

ENEPIG is formed by the deposition of electroless nickel, followed by electroless palladium, with an immersion gold flash. It forms exceptionally robust solder joints with lead-free SAC-type alloys. In extended solder joint testing, shear ball tests indicate zero loss of solder joint strength. SEM studies and elemental analysis shows that the presence of palladium at the joint interface virtually eliminates inter-metallic propagation. It withstands multiple lead-free reflow soldering cycles.

Most fortuitously, ENEPIG, unlike electrolytic processes, has no requirement for bussing lines, which facilitates the design of ultra high-density circuits.

ENEPIG is also not susceptible to grain boundary corrosion. Palladium is plated via chemical reduction, rather than displacement, so there's no opportunity for compromise of the electroless nickel.

Finally, the ENEPIG process is less costly than electroless bondable gold; savings of 80% of the total final finishing cost can be realized when users of electroless nickel gold upgrade to ENEPIG.

Several additional factors led to Micron's specifying UIC ENEPIG – and these factors are also compelling for shops who are contemplating the addition of an ENEPIG line – or replacement of an ENEPIG chemistry that is not performing as expected. Chief among them is Uyemura's proprietary, reduction-assisted immersion bath for board customers who spec a gold deposit above 1-2 µin. Called TWX-40, this ENEPIG component is a mixed reaction bath – an elite hybrid – that produces simultaneous immersion and autocatalytic (electroless) deposition.

TWX-40 is a proven alternative to other attempts to achieve heavier gold deposits on

ENEPIG, i.e. extending the dwell in the immersion bath, or depositing autocatalytic gold over immersion gold. The former damages the nickel underlayer; the latter requires an added step, and costly additional make-up.

TWX-40 has substantially widened the operating window for wire bonding by facilitating the deposition of thicker gold while maintaining the integrity of the underlying palladium and nickel.

TWX-40 is a single immersion gold bath with autocatalytic capabilities that deposits 4-8 µin gold in one step. For ENEPIG users serving a diverse customer universe, it is a proven solution with excellent science behind it.

The other process component widely credited with the success of UIC ENEPIG is Talon. Talon deposits an electroless / autocatalytic palladium that is both solderable and aluminum / gold wire bondable. The bath has a low palladium metal

content and is highly stable. The deposition rate and deposit quality are exceptionally consistent.

A version of UIC's Talon allows palladium to be deposited directly onto copper, aluminum or electroless nickel.

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