Recent Advances in Final Finishes Push Past the Limits of Conventional Electrolytes

In a wide-ranging interview, Uyemura Business Development Manager Rich DePoto explores DIG, RAIG, EPIG, and the competition-fueled evolution from mSAP to full semi-additive SAP.

Please explain DIG and RAIG plating technologies and how they compare with more traditional final finish technologies.

Rich DePoto: Reduction-assisted Immersion Gold (RAIG) is a platform of final finish processes that are the next generation of immersion gold electrolytes. RAIG electrolytes were developed to address three important limitations of conventional immersion gold electrolytes.

1. Tight control of immersion gold thickness.

Conventional immersion gold electrolytes operating under less than ideal process control can produce plated gold that is susceptible to electroless nickel corrosion; in extreme cases this corrosion results in “black pad” reliability failures. ENIG black pad failures are a serious reliability concern and should be prevented at all costs. The IPC 4552 Rev B specification for ENIG limits immersion gold thickness, and includes expanded cross-section measurements inspection to avoid this scenario. For the most part, companies have met the new IPC criteria. However, out-of-compliance situations are an ongoing threat, and the many variations that produce these failures are not always monitored as closely as needed. The implementation of an RAIG immersion gold bath provides a significant enhancement in gold thickness uniformity on a variety of pad sizes and configurations. This tight distribution is evidenced in Figure 1 and the graphs in Figures 2 and 3, where a mean of 2.0 µin with a standard deviation of only 0.226 µin was established.

2. Limitations on immersion gold thickness.

To prevent excess nickel corrosion, the IPC specification requires immersion gold thick-

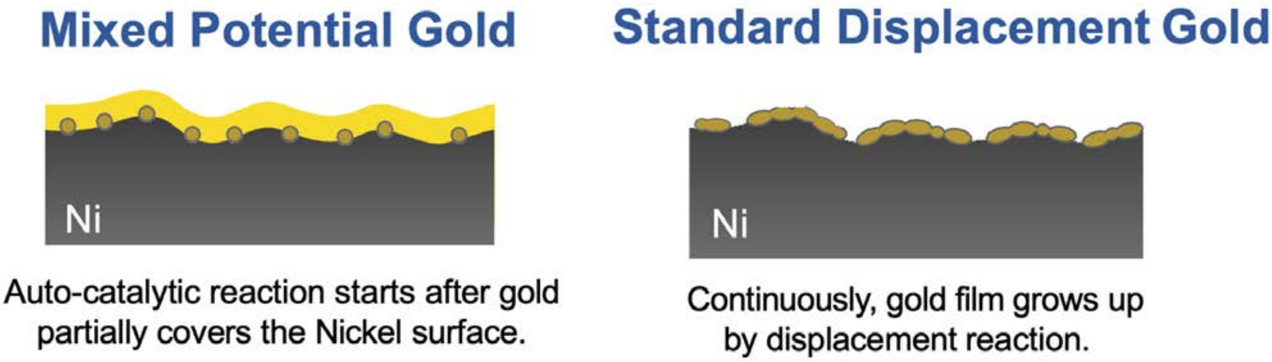
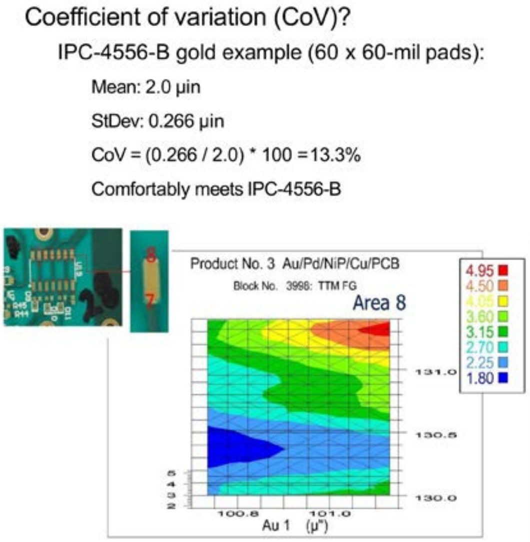


Figure 1: Reduction-assisted immersion gold vs. standard displacement.



Coefficient of variation (CoV)?

IPC-4556-B gold example (60 x 60-mil pads):

Mean: 2.0 µin

StDev: 0.266 µin

CoV = (0.266 / 2.0) * 100 =13.3%

Comfortably meets IPC-4556-B

Figure 2: RAIG performance/deposit variance.

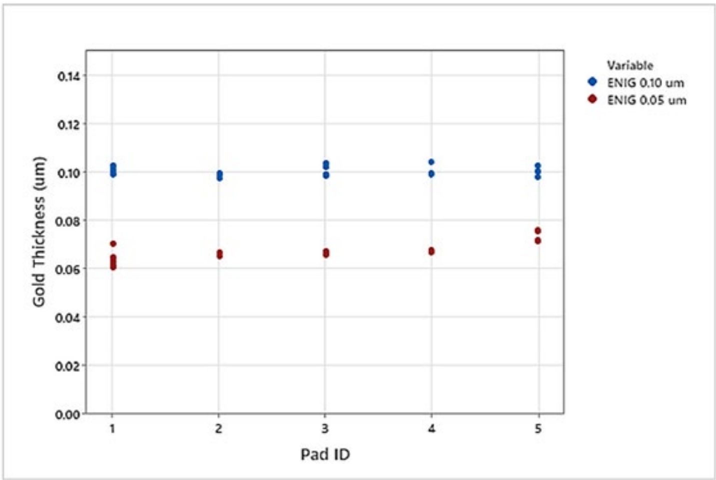


Figure 3: Gold thickness distribution vs. pad ID-ENIG.

ness to be statistically controlled to between 1.5 and 4.0 microinches. Restricting gold thickness to a maximum of 4.0 µin is not ideal for many OEM assembly tasks, including specialty wire bonding, touchpad, and non-soldered pin connection applications. OEMs that specify higher immersion gold thickness often find their designs under deviation or not bid. They continue to request thicker immersion gold and many PWB manufacturers have customer specifications at the upper limit of the IPC spec in their manufacturing queue.

3. Building gold thickness on ENEPIG.

Immersion gold deposition on nickel is a straightforward and strongly-driven electrochemical reaction. Conversely, immersion gold deposition on electroless palladium is a much lower-driven reaction. This results in two undesirable scenarios: slow and inconsistent gold-on-palladium plating rates, and an underlying preferential electroless nickel attack, known as “tunneling.”

RAIG is a mixed potential chemical reaction—a hybrid reaction. The initial gold-nickel reaction is an immersion reaction that is followed instantaneously by an autocatalytic electroless gold deposition reaction. The latter provides the final thickness.

The autocatalytic gold deposition process receives its electrons from a reducing agent, effectively precluding further electroless nickel corrosion. This RAIG feature eliminates the opportunity for excessive nickel corrosion and corresponding IPC corrosion level 111 and black pad reliability issues. This new generation immersion gold plating process is quickly becoming an industry “best practice” and is commonplace in new and upgraded final finish plating lines. As evidenced in Figure 4, RAIG thickness uniformity virtually mirrors that of ENIG in Figures 2 and 3.

An equally important feature of the RAIG process is its ability to plate thicker gold on both electroless nickel and electroless pal-ladium without any risk of nickel corrosion. Specifically, by taking advantage of the auto-catalytic gold reaction, these electrolytes predictably build gold thicknesses significantly above the IPC threshold of 4.0 microinches. The effective range for RAIG thickness is 1.5 to 8.0 microinches, which more than meets the needs of the OEM specialty assembly processes referenced earlier, while allowing the process to be used successfully in mainstream IPC designs. As per the IPC-4552 Rev B specification, it calls out the use of RAIG for thicker gold deposits. Table 1 shows “level zero” nickel corrosion for both ENIG and ENEPIG in RAIG deposits.

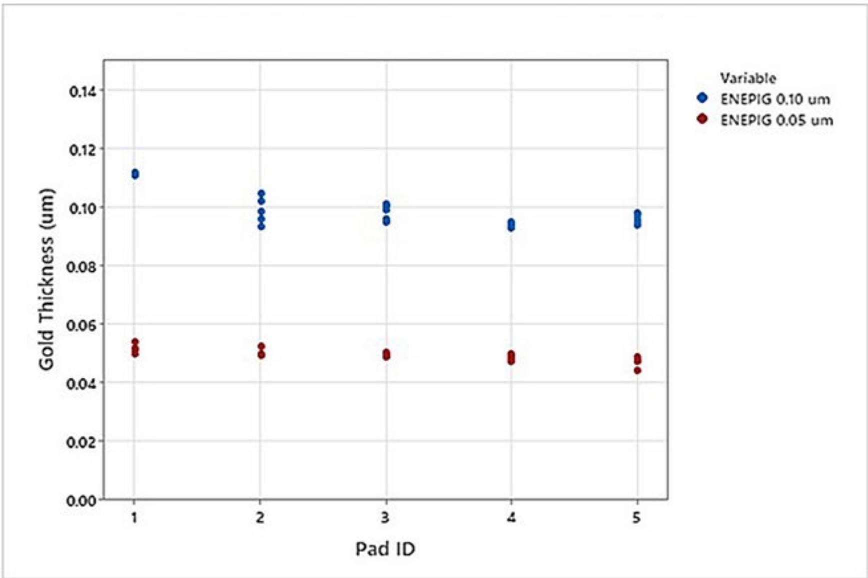
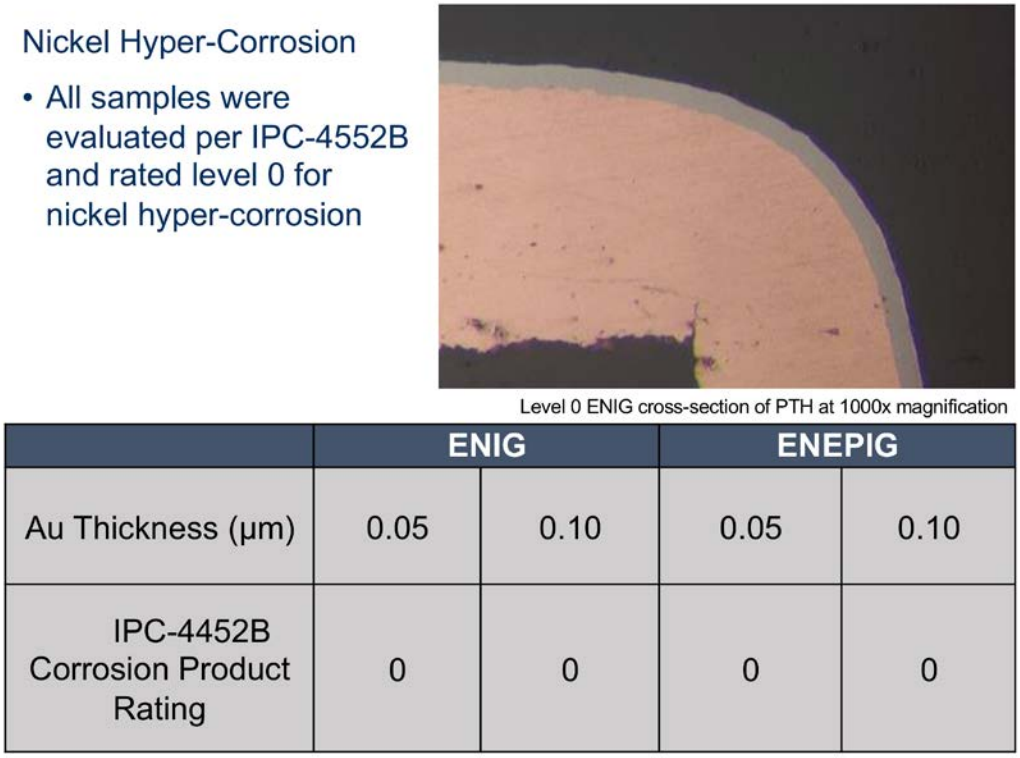


Figure 4: Gold thickness distribution vs. pad ID-ENEPIG.

What applications and PCB technologies are using direct immersion gold?

DIG is a final finish alternative to ENIG. Direct immersion gold is a nickel-free final finish that eliminates electroless nickel from the ENIG deposit stack. The DIG process is a straightforward immersion reaction between copper and gold. By removing the nickel, we eliminate the primary copper diffusion barrier of the final finish stack and extend

Table 1: Nickel hyper-corrosion cross-section



Nickel Hyper-Corrosion

- All samples were evaluated per IPC-4552B and rated level 0 for nickel hyper-corrosion

Level 0 ENIG cross-section of PTH at 1000x magnification

	ENIG		ENEPIG	
Au Thickness (µm)	0.05	0.10	0.05	0.10
IPC-4452B Corrosion Product Rating	0	0	0	0

the shelf life and solderability following multiple soldering operations. Copper atoms readily diffuse through porous gold layers, reducing solderability and increasing contact resistance.

That said, DIG has several notable features:

- The intermetallic during solder assembly is copper-tin, a well-understood and reliable interface. The intermetallic is less brittle than nickel-tin and better suited for applications involving mechanical stress, such as bending and twisting.
- Removing electroless nickel from the deposit stack improves high frequency circuit performance where EN's magnetic properties increase insertion loss and high speed signal attenuation.
- The removal of the nickel is valuable in fine pitch line-and-space design where the thick nickel diffusion layer (200 min) reduces spacing.
- The process is less expensive than the premium final finishes of record: ENIG and ENEPIG.

The DIG process is particularly advantageous for high-frequency designs where assembly processes are less complex, and shelf-life solderability is not a concern. DIG is not suitable for long-term storage and solderless connection applications.

What applications and PCB technologies are using RAIG?

PWB manufacturers with ongoing, high-volume ENEPIG customers benefit most from RAIG because RAIG is particularly well suited to plating consistent thicknesses of gold on electroless palladium. As previously mentioned, the lower electrochemical reactivity of gold and palladium makes the autocatalytic feature of RAIG gold singularly useful.

By building gold thickness on palladium autocatalytically, deposition rates and corresponding thicknesses are optimally uniform and predictable. Overall, RAIG gold deposits exhibit a tighter grain structure, resulting in less gold porosity. It has been noted by a number of OEMs that lower ENEPIG gold porosity increases connection reliability for solderless assembly, such as hydrostatic component connections.

The second instance where RAIG offers a unique and clear advantage is for customers that specify highly reliable ENIG with zero nickel corrosion. Even the highest reliability immersion golds cannot guarantee zero nickel corrosion. OEMs do specify "zero EN corrosion." For many PWB manufacturers, the desire to exceed IPC-4552 Rev B stems from the fact that, in the event of a part failure in the field, the presence of any nickel corrosion will be central to what follows. Even absent definitive causation, this correlation will open the PWB manufacturer to potentially crushing liability. This risk is sufficient for many manufacturers to implement what is considered the best available finish gold technology.

Figure 5 shows an ENIG-RAIG micro-section analysis after the part was exposed to double the normal process dwell time. This is an example of a corrosion analysis of an ENIG part, with a 40-minute dwell time in an RAIG immersion gold bath. Part analysis showed a consistent "level zero" corrosion rating.

The final justification for RAIG is for OEMs that have determined that ENIG gold thicknesses above 4.0 microinches are advantageous for their specific assembly process, potentially improving wire bonding performance or allowing for the use of a specialty contact resistance component. What we know is that thicker gold correlates directly to lower gold porosity. Lower gold porosity provides greater protection against nickel oxidation and better performance in harsh environments. Those two performance features are critical for solderless connections.

Figure 5: Cross-section of corrosion check after 40 minutes of dwell time in immersion Au bath.

What is the cost/benefit argument for moving to either of these processes?

RAIG is a must for the consistent production of high-reliability ENEPIG PWBs. Using RAIG rather than conventional immersion golds will, however, slightly increase the cost of the immersion gold part of the ENIG or ENEPIG process. The main reasons are:

- A typically higher gold content (grams/liter) in the bath at operating conditions
- The useful life of the bath may be restricted if not run frequently
- The electrolyte can plate-out to the tank walls and plumbing more easily

There are, however, considerations relative to RAIG that close the cost gap:

- RAIG for equivalent thickness typically has greater thickness control, which reduces gold usage
- The high consistency of gold plating times when using ENEPIG improves efficiency, process reliability and yield, and lowers rework
- RAIG completely eliminates nickel corrosion on ENIG and ENEPIG work

DIG is less expensive than ENIG and much less expensive than ENEPIG as a final finish. DIG is a more expensive final finish than immersion silver.

DIG is a specialty final finish and not considered a premium final finish because, without the nickel, it has reduced solderability shelf life, but has shown some resistance to multi-

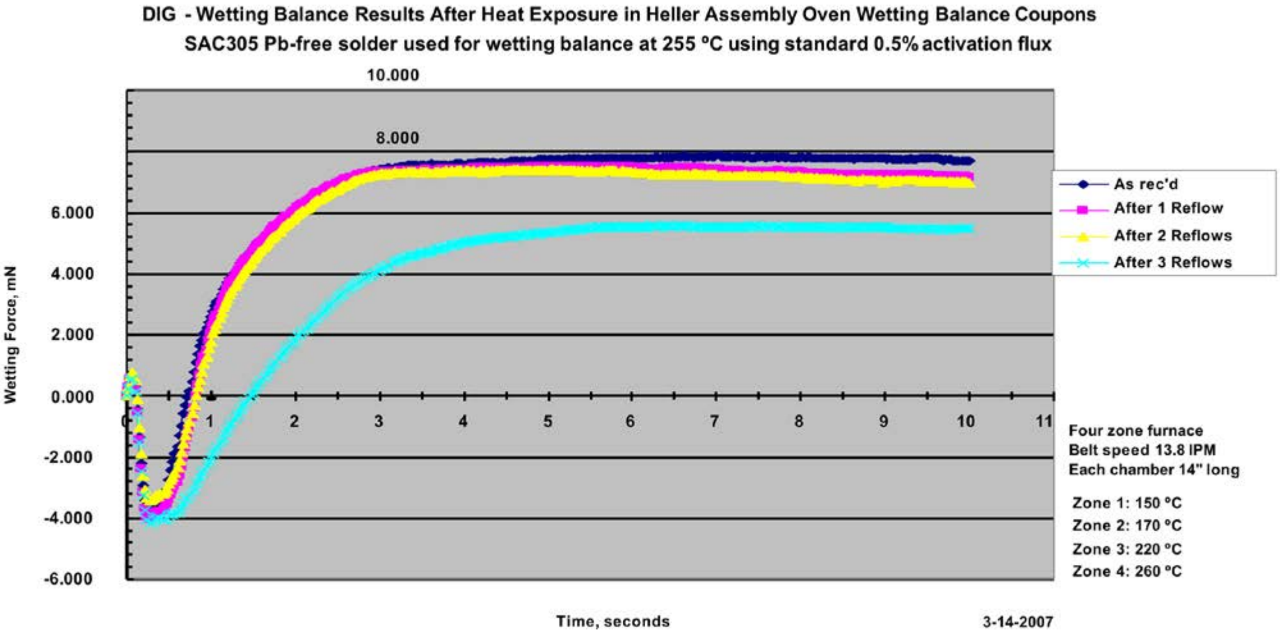


Figure 6: DIG wetting balance results after reflow simulation. No anti-tarnish used

ple soldering operations, as evidenced in the wetting balance graphs in Figure 6. DIG has important advantages as a high frequency final finish for less complex assembly processes. It is a good substitute for immersion silver and has demonstrated compatibility with wire bond-ing. DIG does not appear to be fully compatible with solderless assembly or contact resis-tance connector applications.

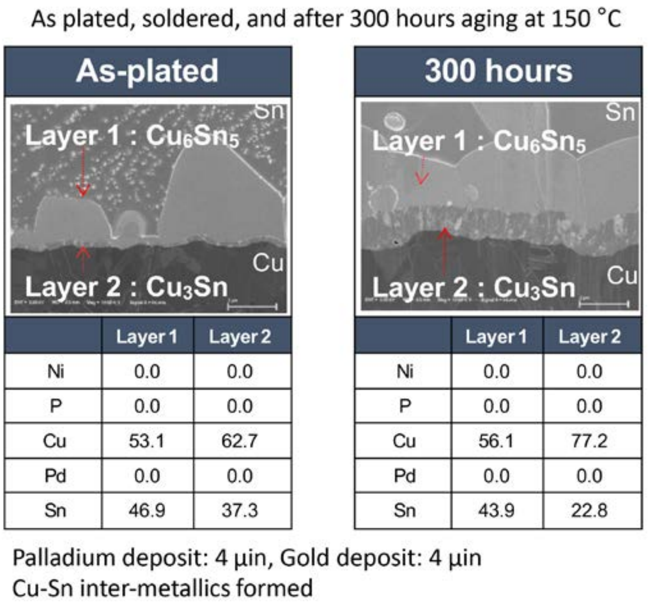
Is Uyemura developing alternative PCB plating technologies?

With respect to final finish alternative processes, we have several products in our commercial portfolio. Most notable are EPIG, EPAG, and IGEPIG, two premium final finish nickel-free electrolytes. These processes are comprised of electroless palladium and immersion/RAIG gold.

The drivers for the nickel-free systems are twofold. The removal of nickel from the stack reduces signal insertion loss and improves the performance of high-speed circuits. High frequency designs are moving well above the 100 GHz speed and preclude the use of magnetic metal deposits.

The second driver is finer densities on trace spacing, which are incompatible with thick nickel plating stacks. The demand for thin, low-porosity palladium deposits that produce an effective copper diffusion layer will be critically important. Table 2 shows the reliability performance of EPIG after stressing for 300 hours at 150°C. Figure 7 shows the wire bonding reliability at different palladium and gold thicknesses. Higher gold thicknesses, for example, allow for thinner palladium depos-

Table 2: Solder joint formed with SAC305 solder



As plated, soldered, and after 300 hours aging at 150 °C

As-plated

	Layer 1	Layer 2
Ni	0.0	0.0
P	0.0	0.0
Cu	53.1	62.7
Pd	0.0	0.0
Sn	46.9	37.3

300 hours

	Layer 1	Layer 2
Ni	0.0	0.0
P	0.0	0.0
Cu	56.1	77.2
Pd	0.0	0.0
Sn	43.9	22.8

Palladium deposit: 4 µin, Gold deposit: 4 µin
Cu-Sn inter-metallics formed

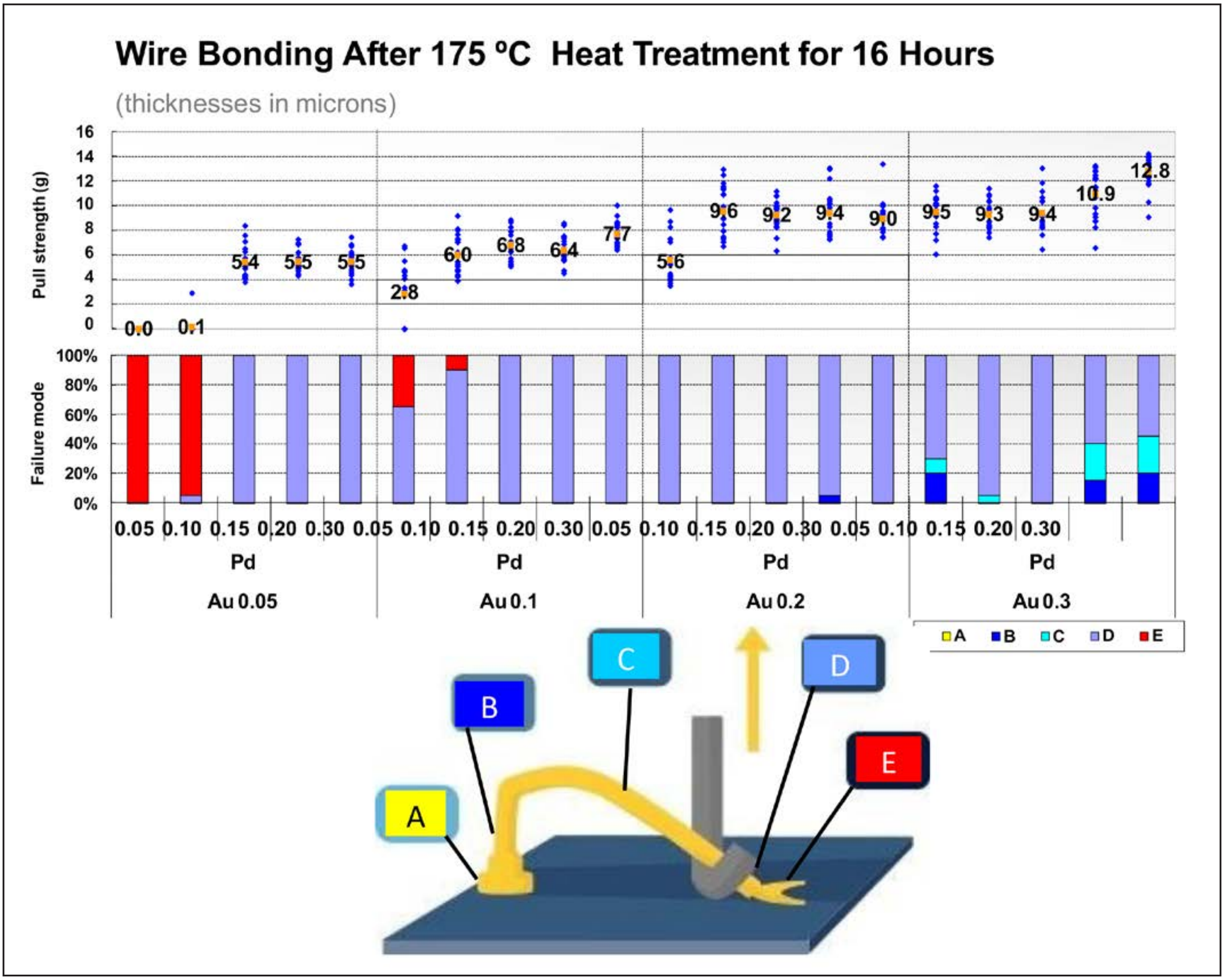


Figure 7: EPIG wire bonding performance using 1-mil gold wire.

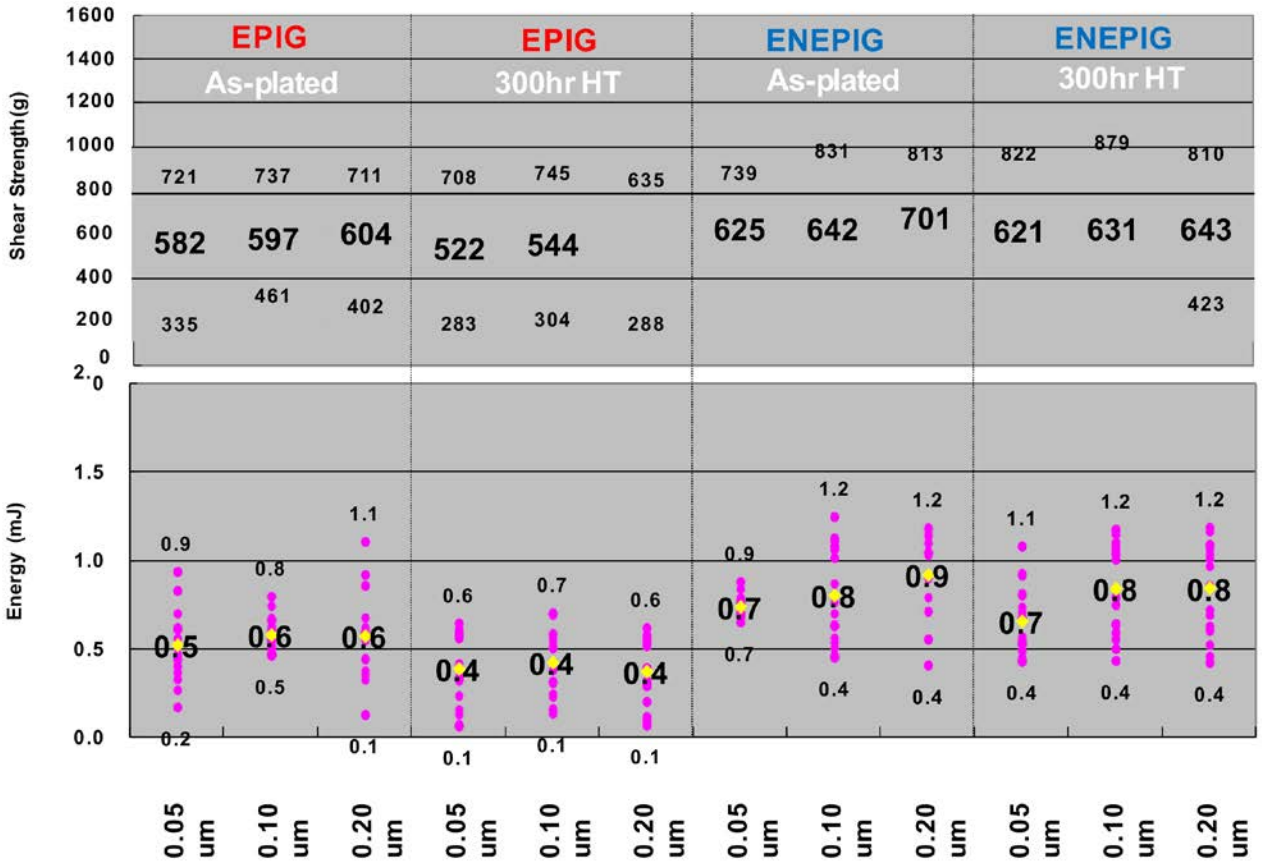
its to be incorporated. Figure 8 shows EPIG performance against the industry standard ENEPIG, which incorporates the nickel layer. We see EPIG performing competitively with ENIG and ENEPIG in this representation.

We are excited to have processes that are well-positioned for the premium nickel-free market, including products with thin, low-porosity palladium diffusion layers. This portfolio fits well with our enhanced RAIG processes, and uses a proprietary reaction to produce a high-reliability, thin and tightly grain structured pure palladium layer.

For the lower cost, high frequency market, the conductivity advantages of our immersion silver are significant; our development lab has made great strides in increasing its overall performance and versatility.

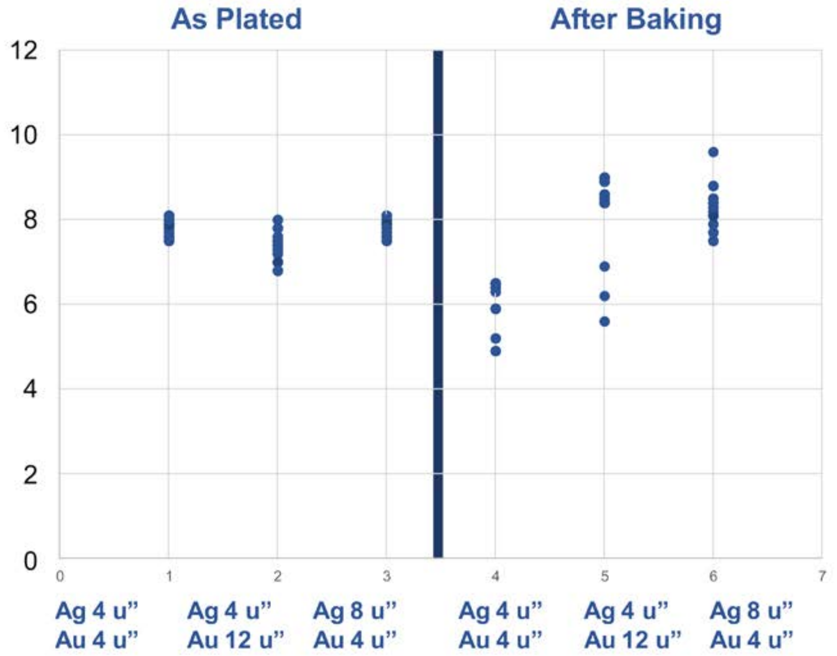
There are also advantages to combining the conductivity, low cost, and simple process flow of immersion silver with an RAIG final finish. This novel deposit stack combines the benefits of silver with the tarnish resistance of a gold overlay. The process dramatically increases shelf life and is compatible with complex assembly processes. These facts, and a low cost, are expanding the landscape for immersion silver.

Figure 9 shows the performance of ISIG in wire bonding as plated and after baking. The wire bond performance is comfortably above specification for this final finish deposit.



As plated: soldered at 260 °C, after soldering followed by 300 hours aging at 150 °C

Figure 8: High speed ball shear test results: EPIG vs. ENEPIG.



1 mil Gold Wire

Baking at 175 °C 16 Hours

All breaks in the wire

No failures at the ball or stitch bond

Figure 9: Gold wire bond results using 1-mil gold wire.

For enhanced DIG capability, we recently introduced a commercially available DIG thick gold, which has extended DIG applications to more complex assembly processes and made the process more compatible with wire bonding operations. We envision companies with new final finishes incorporating this into their overall growth strategies, and using it as an important tool for "future-proofing" their operations.

Is Uyemura currently using sputtering as an application process for any of your plating finishes?

Uyemura does not use sputtering (or vapor deposition) in any of its processes or applications. The major reason is that Uyemura is primarily a specialty chemical solutions provider vs. a metals supplier. Uyemura's mission is to replace processes such as sputtering and vapor deposition with alternative metallization using chemical electrolytes such as plating baths.

Given equal playing fields for performance, history shows that a chemical electrolyte is less expensive and more scalable in cost, efficiency, and productivity. The result is that although sputtering is commonplace, it has serious limitations in scalability, productivity, and long-term cost management. So, we continue to focus on substrate metallization using chemical electrolytes.

Related to chemical electrolyte metallization of substrates used in the PWB and microelectronics industries, we have primarily focused on electroless copper and specialty pretreatment chemicals that improve copper adhesion to organics, filled organics, organo-metallics, composites, and specialty glass substrates. The capability to thinly metallize a variety of substrates, including specialty glass, will help PWB manufacturers move to the next phase of high-density circuitry: HDI and IC substates. We are gratified that today's business climate is encouraging North American PCB investment, including IC substrates facility subsidies.

What should PCB manufacturers be asking when considering moving to or adding direct metallization to replace traditional plating methods?

The most logical strategy is to have an HDI/UHDI strategy roadmap defining separate processes, pursuing evolutionary processes first for 25-micron lines and spaces, then moving to sub-15 micron line and space density.

The limit of an modified semi-additive process (mSAP) based on subtractive PWB manufacturing is between 40 and 25 microns. By gaining experience and process knowledge using a subtractive mSAP process with thin laminated copper-clad substrates, you will be well positioned for evolution to a semi-additive process (SAP) which uses an electroless copper-plated substrate process as the metallization step.

The mSAP process flow is familiar to most PWB manufacturers and will require only a few "carefully placed process enhancements" to achieve prototype capability—and even pilot production.

This experiential learning of first using mSAP will pay dividends for the phase 11 process evolution, which is required for a full SAP process. A full SAP requires plating a thin electroless copper deposit on an unclad substrate; this ultra-thin copper deposit seed layer allows finer lines and spaces with minimal circuit geometry undercut.

A number of the carefully placed process enhancements, as well as the evolution to a full SAP process, will require specialty etching

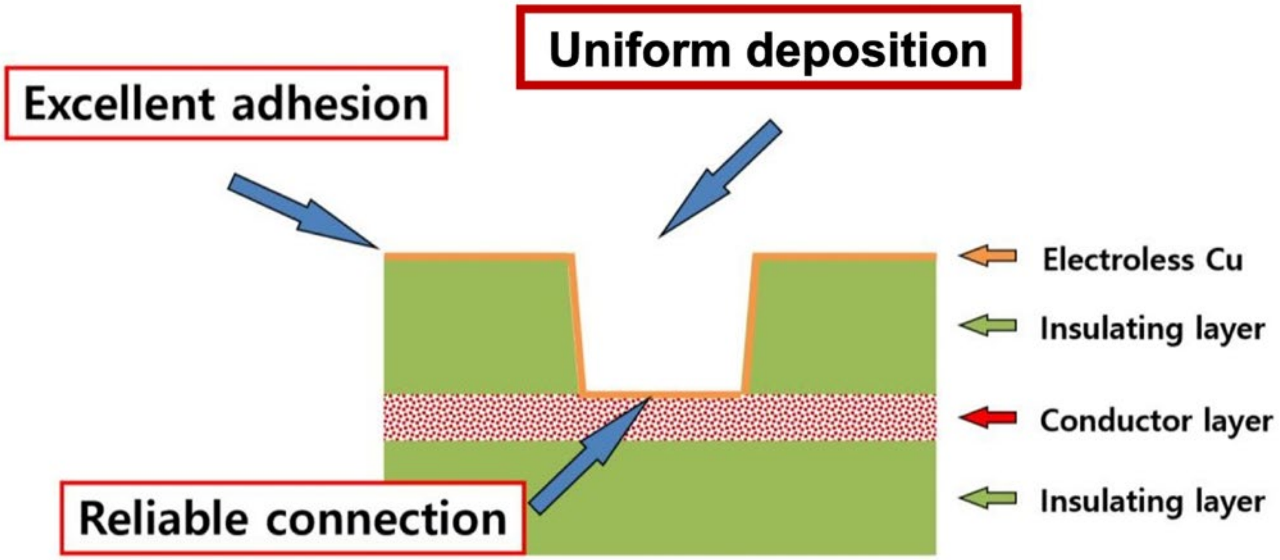


Figure 10: Basic schematic of SAP process and SAP via formation.

chemistries, adhesion promotors (coupling agents), and specialty catalysts to optimize etching geometries, as well as specialty copper "trench/via" plating electrolytes. Uyemura has worked in partnership with MEC etchants to establish a portfolio of commercial products specifically for this application.

Will this become more mainstream in the next decade?

Nearly all the major PWB manufacturers are embracing the technologies discussed here in the next three to five years for these reasons:

- Numerous U.S. companies have already established advanced capability for EPIG, EPAG, DIG, mSAP and, to a lesser degree, SAP. In addition, final finish contract platers are forging ahead toward this capability as a means to qualify new processes and customers.
- These capabilities already exist overseas; they are proven, installed (even automated), and can easily be benchmarked for smooth technology transfer.
- As a specialty chemical company, we routinely participate in equipment design reviews, so we see the majority of new equipment orders incorporating the advanced technologies we've discussed into their equipment specifications and purchases.
- Electrical design engineers continually expand their high RF thresholds above 40 GHz. This is where nickel-free final finishes begin to deliver unique performance advantages.

The PWB roadmap for HDI, UHDI, and IC substrates will initially use an mSAP process strategy for advanced fine-pitch circuit designs, prompting a partial shift from ENIG/ENEPIG to EPIG/EPAG for high frequency designs. Once PWB manufacturers are comfortable with modified SAP (mSAP), the move to full semi-additive SAP will occur quickly. The timing for each company will depend on their respective competitive ambitions, acceptable yield thresholds, and customer require-ments. The basic schematic structure for SAP is shown in Figure 10.

Rich DePoto, Chemical Engineer and Business Development Manager at Uyemura International, works with OEMs and PWB fabricators on advanced final finish strategies for HDI and IC substrates. He leads an HDPug consortium on final finishes and glass substrates.