Blind vias that connect layer 1 to layer 2 or layer 3 are an enabling technology for HDI-type boards. Via fill makes for a robust connection (Figure 1) with no chance of any voids during assembly. Vias with 1:1 aspect ratio are common.

Successful via-fill plating requires a specific electrolyte; the copper concentration is high at 50–60 g/L copper with low sulfuric acid at 30–60 g/L. This is combined with a unique organic additive combination with a prominent leveling component. The leveling component acts predominantly on the surface and suppresses the surface plating allowing the brightener and carrier combination to plate up from the bottom of the via. Ideally the solution movement must be vigorous and parallel to the surface (laminar flow); this ensures adequate leveler replenishment.

The mechanism of via filling is different from through-hole plating. A good understanding of the following influencing factors is paramount to the success of the process.

**The Electrolyte**

The electrolyte is composed of inorganic and organic components. The inorganic component for via fill is primarily a high-copper low-acid system. This ensures that there is no shortage or depletion of copper ions anywhere on the plating surface. The organic additives are composed of three components, namely the carrier or suppressor, the brightener or accelerator, and the leveler which is a selective suppressor.

Carriers increase the polarization resistance and are current suppressors. The suppression is a result of the carrier being adsorbed to the sur-
face of the cathode; this results in increasing the effective thickness of the diffusion layer. The result is better organization. This gives rise to a deposit with a tighter grain structure. The carrier-modified diffusion layer also improves plating distribution without burning the deposit.

The brightener is a grain refiner. Its random adsorption produces a film that will suppress crystallographic differences. The brightener produces a fine-grained, non-directional (equiaxed) grain structure. It is the additive that directly affects the tensile strength and elongation properties of the deposit.

Levelers are small molecules that carry a partial charge that are attracted preferentially to the higher current density areas on the plating surface. Levelers, or leveling agents, are selective inhibitors present at low concentrations in the electrolyte, as compared to the depositing metal. Vigorous solution movement is required to replenish the leveler at the surface of the panel. Figure 2 shows an example of a mis-located air sparging pipe resulting in vigorous solution movement on the filled side with hardly any movement on the voided side.

Maintaining the organic additives within the recommended operating window is critical to the success of the process. This is accomplished by establishing a dosing system that is triggered by an ampere-hour accumulator. The additives are analyzed using cyclic voltametric stripping (CVS) analytical techniques.

**Filling Mechanism**

There are multiple concurrent mechanisms that take place for the via-filling process to occur. The brightener and the carrier are evenly distributed throughout the via and their combined effect is to promote plating. The leveler component is only active at the knee of the hole (high current density area). It inhibits the plating at the via entrance which helps to keep the via open, allowing the brightener/carrier combination to preferentially plate up the bottom of the via. Refer to the progress of plating in Figure 3. Replenishment of the leveling component at the copper surface is a function of solution movement. Vigorous laminar flow across the surface must be designed in the original setup. In the absence of the leveler effect, the knee of the via would plate at an accelerated rate, closing the via before the filling is complete (Figure 4).

This same mechanism can fill a small diameter, low aspect ratio through-hole like a 6.0-mil diameter hole in a 10-mil thick laminate.

**The Plating Cell Setup**

The plating cell design is not that different from standard acid copper plating. Attention must be made to ensure adequate anode cathode spacing (7–12 inches) in the initial design. The plating cell must be equipped with temperature control capabilities, mostly cooling. An overflow weir is recommended to maintain solution level and to facilitate filtration of suspended particles. Filtration thru 5–10 micron filter cartridges should be continuous and designed at a flow rate to ensure a minimum of two solution turnovers per hour (>2 STO). The filtration system draws from the bottom of the weir and returns below the cathode.

The number of anodes (usually titanium baskets filled with copper balls) should be optimized for the platable area of the cathode; maximum for panel plate and minimum for dot pattern (pads only). Anode placement should be such that the active length of the anode is 3–4

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*Figure 2: Misplaced air sparger; solution movement only on one side (filled vias).*
inches shorter than the cathode, and should be tucked in 3–4 inches inside the cathode window on the outside vertical edges.

The panels ideally should have a common vertical dimension and should be racked with minimum gaps. If the cathode bar is not fully racked, dummy panels or thieving strips must be used to prevent imbalance in thickness distribution; alternatively the anode baskets opposing the gap may be isolated.

Figure 3: Preferential bottom plating in progress.

Figure 4: Conformal plating.

Figure 5: Schematic of plating tank configuration.
Solution agitation is initiated at the bottom of the tank; it may be air sparging or eductor agitation. There should be two manifolds, one in front of the panel and one in the back. The spacing between the top of the sparging system and the bottom of the panel should be at least six inches. It is intended to produce a uniform laminar flow across the surface of the panel. The flow should be vigorous to ensure sufficient leveler replenishment at the entrance of the via. Via filling will not occur if solution agitation is inadequate as demonstrated in Figure 2. Part agitation is not necessary in this setup.

**Rectification**

The rectifier should be sized to supply the desired output. For example if the platable area is limited, a smaller rectifier would be the right choice, it is not advised to use a 200 ampere rectifier to plate at 10–20 amperes per load. Ripple (% AC or alternating current) should be less than 5% to ensure the deposit is fine-grained, adherent and equiaxed. High ripple would have an adverse effect on the physical properties of the deposit. The rectifier control accuracy or resolution should be 1–2% to ensure consistency of output.

The ASF to be used in plating the blind via should be optimized for the via dimensions. More demanding vias (higher aspect ratio) will require lower ASF for a longer time. Traditionally there are two approaches to the plating current density (CD). The first approach is a single CD for the duration of plating. The second approach is to step up the CD with time, for example, 10 ASF for 45 minutes followed by 20 ASF for 30 minutes and then 25 ASF for 15 minutes. Both methods work and the choice should be made at the initial installation through experimentation and testing. Once established, this becomes the method. The method may be optimized again as the next level of difficulty (higher aspect ratio) is encountered.

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**Figure 6: Variation in current density distribution in “dot” pattern plating.**

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Panel vs. Pattern Plating

Both methods of plating are being utilized in the industry. Panel plate creates greater uniformity across the board; however, it is more demanding on the planarizer to reduce the plated surface copper. Flash plating the electroless copper is not recommended as it tends to increase the aspect ratio of the hole.

In most cases pattern plate is a pads-only pattern, referred to as a “dot” pattern. The panel after electroless metallization is imaged using photoimagable dry film resist. A half inch of non-imaged laminate copper is left exposed on all four sides. This edge is used for rack connectivity during electroplating. This copper edge has a thieving effect on the distribution of the copper thickness above the via. Vias or pads in the center of the panel will plate much thicker than their counterparts closer to the edge. Figure 6 shows that the current density at the different locations varies more than 2X between the vias along the edge versus the vias in the center of the panel; note that all the vias are filled in spite of the large variation in current density from via to via. All the variability in copper thickness above the via is removed during planarization.

Periodic carbon treatment, to remove organic contaminants leaching from the dry film, must be set up on a regular basis to ensure consistent performance from the electrolyte.

Pre-treatment

The pre-treatment is composed of the following steps: cleaner, micro-etch and acid pre-dip.

Figure 7: IPC-6012D, filled via plating requirements.
The Cleaner Step

The cleaner is composed of a solvent, an acid and a surfactant. The solvent removes organic surface residues by dissolution. The acid removes oxidation and the surfactant wets the surface. The wetting is very important when plating small high-aspect ratio holes or blind vias; a well wetted surface will not entrap air. Intermittent vibration in this step is helpful to ensure that all air is dislodged from tight spaces. Follow vendor’s recommendations of concentration, temperature, dwell time, and dump and remake schedule to ensure the cleaner functions as intended. Good two-step rinsing is important after the cleaner as its components in trace amounts, if dragged down the line may adversely affect the plating.

The Micro-etch Step

The micro-etch is made up with a strong oxidant like sodium persulfate or hydrogen peroxide in a sulfuric acid medium. The micro-etch oxidizes the surface copper and literally etches it away, exposing a fresh copper surface for plating. If the metallization used is electroless copper; the concentration and dwell time should be controlled to ensure that the electroless copper is not etched away. In addition, the micro-etch can undercut minute stubborn residues that the cleaner did not remove. Concentration, temperature, dwell time, and dump/remake schedule must be adhered to. The panels are double-rinsed after the micro-etch.

The Pre-dip Step

The pre-dip is made up with sulfuric acid at 5–10%. This step ensures that the surface is oxidation-free and is acidic to match the acidity of the electrolyte. There is no rinse between the pre-dip and the acid copper bath.

Voids

Ideally there should be no voiding in the copper-filled via. The latest version of IPC-6012D spells out acceptability criteria as detailed in Figure 7.

The primary cause of voids is poor wetting of the via by “entrapped air.” All air must be removed from the via in the initial cleaner step. Cleaners with low surface tension are better suited for this task. Intermittent vibration in the cleaner ensures that all air is dislodged and that the surface of the via is fully wetted. Figure 8 demonstrates air entrapped voiding.

Another form of voiding occurs when the plating at the knee of the via proceeds at a faster rate than at the bottom (Figures 2 and 4). Here the hole is closed at the entrance before the bottom plating has filled in. This is the result of imbalance in the leveling component, poor solution agitation or both.

With a good understanding of the plating principles of the process, proper choice and control of the chemical process, periodic carbon treatment, and paying attention to the details of cell design, the “via fill” process can run trouble-free.

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