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# Via Plating for PWBs

Vias are an integral part of PWB design and manufacturing. They are the means by which different layers of a board are connected. There are three main types of vias: through-hole vias, buried vias, and blind vias.

Through-hole vias are drilled from the top layer through the bottom layer. In a double-sided PWB, the through-hole via connects the top and bottom layers. In multilayer boards (MLBs), the through-hole via is the means of connecting all or any of the layers to meet the design requirements. The desired connectivity occurs when the via is electroplated.

Before electroplating, drilled vias are desmeared and rendered conductive. Desmear–using chemical means or plasma–removes all traces of dielectric residues from the interconnect surfaces to ensure intimate connectivity. Electrical continuity is achieved by rendering the dielectric conductive using metallization like electroless copper or other means like carbon or a conductive polymer. The electroplated copper is the conduit that all signals travel through. This column will address the electroplating of vias (Figure 1).

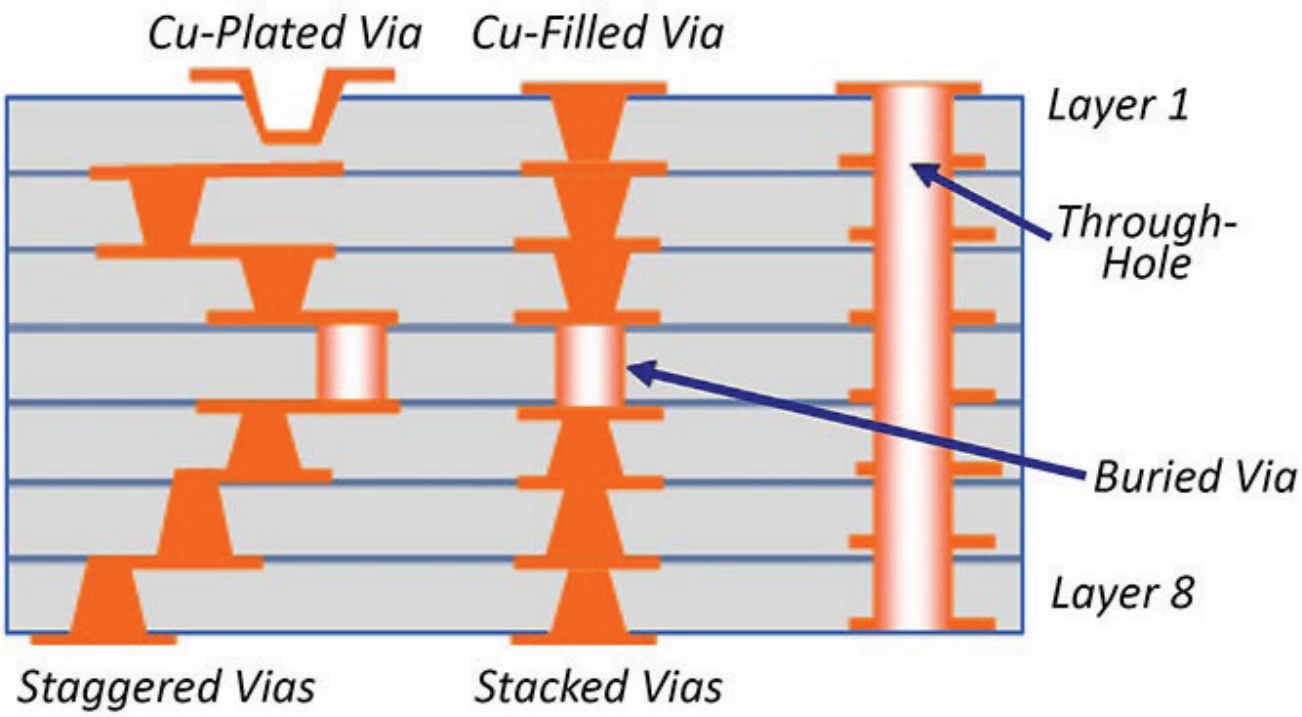


Figure 1: Via types used in PWBs

**Through-Hole Vias**

Through-hole plating remains the backbone of PWB connectivity. The objective is to plate a uniform copper layer that connects the different layers. Connectivity is the key attribute here, whether it is only connecting two layers (top and bottom) or connecting 40 layers in a multilayer board.

The plated copper should be able to withstand 6X thermal shock simulating the stresses that the board may encounter during assembly and through its normal useful life. It should also be able to withstand IST thermal cycling test where stress is induced by the expansion and contraction of the dielectric along its Z-axis. Thickness uniformity of the plated copper must be controlled to ensure the current-carrying capacity of the conduit and to meet its impedance requirements.

For electroplated copper to meet these requirements, the plating process must be optimized. Areas for optimization include:

1. Pretreatment
2. Pattern vs. panel plate
3. Plating chemistry
4. Plating cell setup
5. Agitation
6. Rectification

**1. Pretreatment**

Pretreatment is part of the plating process. It ensures that no air entrapment occurs in high aspect ratio holes and removes organic residues and oxidation. Pretreatment was discussed in detail in last month's column titled "The Critical Role of Pretreatment for Plating."

**2. Pattern vs. Panel Plate**

Pattern plate plates the via and the traces after imaging. This makes the etching for circuitization much less demanding, as it only involves etching a thin uniform layer of the original laminate copper. However, the thickness of the plated copper varies with the pattern. Dense pattern areas plate less than isolated areas. In panel plate, uniformity of thickness is easily achieved. Etching for circuitization is more challenging, particularly in fine patterns, as it involves etching a much thicker layer combining the laminate copper as well as the plated copper. Manufacturers make a choice between panel and pattern plate based on their product mix and their type of equipment/process capability.

**3. Plating Chemistry**

Choosing the chemical system plays a major role in the quality of plating—namely the throwing power and the grain structure. Chemistries low in copper and high in acid have better conductivity and better throwing power. The physical properties of the copper—namely tensile strength and elongation (T & E) — are a function of grain structure. Fine equiaxed grain structure produces the desired T & E, in contrast with a columnar structure that will always fail T & E testing. Grain structure is controlled by the organic additive package (brightener, carrier, and leveler).

**4. Plating Cell Setup**

The plating cell setup must be optimized. This includes anode/cathode spacing, as well as the number and placement of the anodes. This has a direct impact on thickness distribution and uniformity, particularly when coupled with protecting the outside edges of the cathode window through thieving and/or shielding.

**5. Agitation**

Agitation is achieved through the solution as well as part agitation. It replenishes the chemistry at the plating interface and must be optimized for the type of product and the current density of plating. Part agitation is either through-hole or knife edge. Both are effective, but through-hole is more common for hole plating.

Solution agitation may be achieved with air sparging or eductor mixing. Air sparging initiates from the bottom of the cell and is intended to move solution across the surface of the cathode. Eductors may be placed horizontally in the bottom of the tank or on vertical manifolds. In the former, the flow is laminar to the panel, and the latter offers direct vertical impingement. The number of nozzles and their location must be designed to achieve the desired outcome.

**6. Rectification**

Plating occurs when current is applied to the plating cell through a rectifier. The amount (weight) of copper plated is directly proportional to the current and the time. In DC plating, the current (amps per square foot, or ASF) and time must be set to achieve the desired amount of copper to be plated. For throwing power, lower ASF for extended time gives the best results.

An alternative to DC plating is pulse plating. Pulse plating requires a special rectifier that can switch modes from forward to reverse. Although pulse has shown good results in improving throwing power, it is more complex in setting up, as a specific pulse wave may work well for a certain part number but may need to be modified for a different part. Setting up a pulse wave is fairly involved and requires engineering intervention. In addition, the finished grain structure (coarser than DC plating) on the surface may not be ideal for subsequent surface finishing and may create signal loss in high-frequency (>15 GHz) RF applications.

***Common Defects in Electroplated Through-Holes***

If the plating setup is not optimized, common defects may include:

1. Cracking in the plated copper under thermal shock. This is a function of grain structure and excessive dielectric Z-axis expansion and contraction.
2. Post separation between the plated copper and the inner layer. This defect is seen after copper plating; however, its source is usually incomplete smear removal and/or inadequate pretreatment.
3. Voiding that results in non-continuity in the barrel of the hole. This is usually corrected in the pretreatment cycle by eliminating entrapped air in high aspect ratio holes.
4. Dog-bone formation, meaning excessive plating at the knee and the surface as compared to the barrel of the hole. This is corrected by choosing and setting up a “leveling” chemical additive system and reducing ASF with a proportionate increase in plating time.

**Plating Blind Vias**

Blind and buried vias are extensively used in high-density interconnect (HDI) PCBs. Blind vias, in general, connect layer 1 to layer 2. In some designs, the blind via may connect layer 1 to layer 3. Incorporating blind and buried vias allow for more connections and higher board density required for HDI PWBs. They deliver benefits, such as increased layer density in smaller pitch devices, coupled with improved power delivery. The hidden vias help keep the board light and compact. It is common to see blind and buried vias designed in sophisticated, lightweight, higher-cost, electronic products like cellphones, tablets, and medical devices (Figure 2).

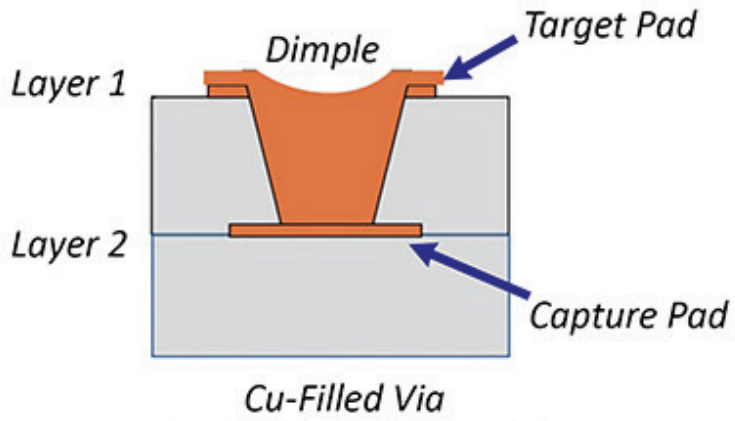

Figure 2: Schematic of a filled blind via.

Blind vias are formed using controlled depth drilling or laser ablation. The latter is the more common method in use today and is usually followed by plasma cleaning to remove any organic residues left after laser ablation. Stacking of vias is manufactured through sequential lamination. The resulting vias may be stacked or staggered, adding extra steps to manufacturing and testing, which come with added costs.

The formed vias may be plated or filled. Plated vias are plated in the same chemistry that is used for through-hole plating. Filled vias require a special chemical system. The system is based on high copper and low acid, coupled with a special organic additive system designed to suppress the surface plating, allowing the plating to proceed from the bottom of the hole to the surface, thus filling the via.

Similar to through-hole vias, optimizing the buried via plating process includes the same six steps as follows.

**1. Pretreatment**
The same basic concepts as with through-hole vias hold true here.

**2. Pattern vs. Panel Plate**
Pattern plate for blind vias is also referred to as dot pattern. The only platable areas after imaging are the pads (dots) around the vias. There is no circuit pattern. In most cases, the pads are all of the same geometry; however, their location relative to the edge of the pattern varies. The surface of pads in the middle of the panel plate higher than pads closer of the pattern edge, where approximately one-half inch of laminate copper is left exposed for connectivity. It is not uncommon to planarize the surface of the plated vias after resist strip. Panel plate is more uniform in surface thickness from pad to pad. However, the added thickness of the plated copper poses its own challenges at etching.

**3. Plating Chemistry**
The plating chemistry for blind via plating is dramatically different from through-hole chemistry. Here, the electrolyte is based on high copper concentration coupled with low acid. The organic additives are a different combination of brightener, carrier, and leveler with emphasis on the role of the leveling component that plays a key role in keeping the edges of the via (the knee) from overplating, closing the via before complete filling, resulting in a void.

**4. Plating Cell Setup**
The plating cell setup must be optimized for via fill. This includes anode/cathode spacing, as well as the number and placement of the anodes. This has a direct impact on thickness distribution and uniformity.

**5. Agitation**
Solution agitation must be designed to ensure the delivery of the different organic/additive components where they are most effective. Solution agitation may be achieved with air sparging or eductor mixing. Air sparging initiates from the bottom of the cell and is intended to move solution across the surface for the cathode. Eductors may be placed horizontally in the bottom of the tank or on vertical manifolds. In the former, the flow is laminar to the panel, and the latter offers direct vertical impingement. The number of nozzles and their location must be designed to achieve the desired outcome.

**6. Rectification**
DC plating of blind vias must be designed for hole filling. It is usually lower current density and longer time than through-hole plating. To improve productivity, the plating ASF may be increased with the filling progression.

***Common Defects in Electroplated Blind Vias***
Separation at the interface of the filled via and the catch pad may occur during IST thermal cycling. This is more common in stacked vias as compared to staggered vias. In a stacked via configuration, the Z-axis expansion and contraction are cumulative to the whole stack and may cause separation at the weakest catch pad interface. In a staggered configuration, although Z-axis expansion/contraction does occur, it is not cumulative and has a much better chance for continuity. A staggered configuration is proven to be more reliable than the stacked one.

Plating voids could also occur during via filling. This is a result of via closure prior to complete filling. This is corrected by optimizing the leveling effect of the electrolyte, which involves the leveler additive concentration and its delivery at the surface through solution agitation.

A dimple (a dish down on the surface of the filled via) may occur. It is a sign of incomplete filling and is corrected by modifying the plating cycle or by plating more copper. Dimples are eliminated during the planarization step.

**Conclusion**
A lot goes into setting up electroplating for through-hole or for blind via plating. The key is optimizing the existing equipment to the parts that are being produced. Revisiting and reoptimizing the plating process must be periodically examined and updated as the product mix evolves.

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